Specification Amendments

Please amend paragraphs [0009] and [0013] of the published application as follows:

[0009] An embodiment of a computing device is shown in FIG. 1. The computing device may comprise one or more processors 100 coupled ~~and~~ to a chipset 102 via a processor bus 104. The chipset 102 may include one or more integrated circuit packages or chips that couple the processor 100 to a main or system memory 106, an audio controller 108, and/or other components 110 of the computing device. In particular, the chipset 102 may comprise one or more device interfaces 112 to support data transfers to and/or from other components 110 of the computing device such as, for example, BIOS firmware, keyboards, mice, storage devices, network interfaces, etc. via one or more buses 114.

[0013] The audio controller 108 may be integrated into the chipset 102. However, in the depicted embodiment, the audio controller 108 is separate from the chipset 102. In such an embodiment, the chipset 102 and the audio controller 108 may each comprise one or more bus interfaces 130 that support isochronous data transfers across isochronous channels 132 and/or non-isochronous data transfers across non-isochronous channels 134. In one embodiment, one or more isochronous channels 132 couple a bus interface 130 of the audio controller 108 to a bus interface 130 of the chipset 102 to support isochronous data transfers therebetween. In one embodiment,

each bus interface 130 may implement a PCI Express compatible interface that supports isochronous virtual channels. However, the bus interface 130 may implement additional and/or alternative interface protocols. Further, the chipset 102 and bus interface 130 may implement ordering rules similar to PCI Express ordering rules that are more lax than conventional PCI ordering rules. In particular, unlike PCI ordering rules, completion data for processor reads might not push isochronous reads and/or writes to system memory 106. Further, interrupts might not push isochronous reads and/or writes to system memory 106. However, in one embodiment, the ordering rules ensure that isochronous writes do not pass previously issued isochronous reads and/or writes across the same channel. ~~FIX-ME: ARE THESE ORDERING RULES ACCURATE?~~